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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/801,809

03/15/2004

Laszlo Hars

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10/01/2007

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION  
INTELLECTUAL PROPERTY & STANDARDS  
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SAN JOSE, CA 95131

EXAMINER

YAARY, MICHAEL D

ART UNIT

PAPER NUMBER

2193

MAIL DATE

DELIVERY MODE

10/01/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/801,809

Applicant(s)

HARS, LASZLO

Examiner

Michael Yaary

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,7-12 and 17-20 is/are rejected.
- 7) ☒ Claim(s) 3-6 and 13-16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1-20 are pending in the application.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims, particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 9 recites the limitation "the NAND gates" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 7-12, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (US Pat. 5,570,307) in view of Fujita et al. (hereafter Fujita)(US Pub. 2003/0061250) and in view of Schultz (US Pat. 4,905,176).
6. Fujita and Schultz were cited in the previous office action dated 05/02/2007.
7. **As to claims 1 and 11**, Takahashi discloses a plurality of groups of independent flip-flops, at least some of the groups having different connection configurations (Column 4, lines 31-44 disclose a plurality of blocks containing flip-flops, and teaches no requirement that the number of flip-flops be equal or even. Thus, the connection configurations could be different among the blocks of flip-flops.).
8. Takahashi does not disclose an exclusive –or (XOR) network connected to all of the outputs of the plurality of groups of flip-flops, wherein a metastable output of at least one flip-flop of the plurality of groups of flip-flops causes a random signal to be output by the XOR network for number generation.

However, Fujita discloses an exclusive –or (XOR) network connected to all of the outputs of the plurality of groups of flip-flops (UFF outputs each connected to XOR in figure 18A), wherein a metastable output of at least one flip-flop of the plurality of groups of flip-flops causes a random signal to be output by the XOR network for number generation ([0049], lines 1-9; [0050], lines 1-4; [0056], lines 1-10; and [0084], lines 1-7).

9. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Takahashi, by implementing an XOR network connected to the flip-flop outputs and implementing a metastable output of at least one flip-flop, as taught by Fujita, for the benefit of efficiently obtaining a random digital signal with a much more compact circuit.

10. Takahashi and Fujita do not disclose a latch connected to the output of the XOR network. However, Schultz discloses a latch connected to the output of the XOR network (latch 26 of figure 4).

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Takahashi and Fujita, by connecting a latch to the XOR output, as taught by Schultz, in order to sample the random signal at low frequency.

12. **As to claims 2 and 12**, the combination of Takahashi, Fujita, and Schultz, disclose wherein the groups of flip-flops are divided into at least three equally sized groups (Fujita discloses five groups of flip-flops in figure 18A).

13. **As to claims 7 and 17**, the combination of Takahashi, Fujita, and Schultz, disclose the groups of flip-flops comprise unequal numbers of flip-flops in each group (Takahashi, column 4, lines 33-38).

14. **As to claims 8 and 18**, the combination of Takahashi, Fujita, and Schultz, disclose delay devices connected within each of the groups of flip-flops have different delay values (Schultz, column 6, lines 41-49).

15. **As to claims 9 and 19**, the combination of Takahashi, Fujita, and Schultz, disclose at least some of the NAND gates are implemented with Boolean equivalents of NAND gates (Fujita, [0116], lines 1-7).

16. **As to claims 10 and 20**, the combination of Takahashi, Fujita, and Schultz, disclose the groups of flip-flops are arranged into one of thirds or fifths (Fujita discloses the flip-flops are divided into 5 groups in figure 18A).

***Allowable Subject Matter***

17. Claims 3-6 and 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

18. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Yaary whose telephone number is (571) 270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2193

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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